

REMARKS/ARGUMENTS:

Claims 1-22 are pending in this Application, claims 21-22 being added herein. In the Office Action dated December 14th, 2004, the Examiner has objected to the Drawings, specifically, to Figures 2A, Figure 1, and Figure 3B. Formal drawings are herein submitted, of which four drawing sheets are corrected pages. Specific corrections are recited above on the page entitled "Amendments to the Drawings". No new matter is added, and this Amendment is seen to overcome those objections.

The Examiner has further objected to informalities in the written description, which are addressed above at the page entitled "Amendments to the Written Description", and this Amendment is seen to overcome those objections.

The Examiner has further objected to claims 1-8, 18 and 20 for various informalities. These claims are amended to comply with the Examiner's suggestions with the following exceptions:

- The term "k" in claim 8 is not replaced, as to re-use the index n as suggested by the Examiner would appear to render the claim indefinite; lowercase n is an index that is upwardly bounded by a predetermined term, which in claim 8 is the integer k. This is consistent with page 12, line 1 of the written description, where it is recited that n=0, 1, 2, 3, ...max. Like "max" in the written description, the term "k" in claim 8 is merely the upward bound to the index "n".
- The term "as data clock" in claim 18 is not replaced with the term "the data clock" as suggested, because such replacement would rely on the claim preamble for antecedent basis. The Applicant elects that the claim preamble provide context for the claimed matter but not limit the claim scope. Drawing antecedent basis from the preamble generally renders the preamble a limiting element of the claim, which the Applicant contends is not warranted given the allowability of the subject matter.

The Applicant notes that certain of the amendments to overcome informalities are not done for reasons related to patentability. For example, deleting the term "further" is seen as non-narrowing and reflective of the Examiner's grammatical preference, to which the Applicant defers. The term "the step(s) of" is deleted in claims 1-8 to avoid the implication that the recited elements must be performed in the exact sequence listed, and is seen as a broadening

amendment. Where one claim element necessarily occurs subsequent to another, the relative order is indicated by a term recited in the later-performed element drawing antecedent basis from the earlier-performed element.

The Examiner has rejected claims 14-19 under 35 USC § 112, first paragraph, for failing to comply with the enablement requirement. Claims 14-17 are directed to an integrated circuit and claims 18-19 are directed to a program storage device readable by a machine. As to claims 14-17, the various claim elements clearly recite circuitry for performing the recited functions. One skilled in the IC arts would be able to make such circuitry on an integrated circuit using ordinary skill as informed by the present specification. For example, one skilled in the art would be capable of forming a binary 2^n PN code generator; such were common at the time of the invention as admitted in the paragraphs beginning at page 1, lines 8 and 18. Similarly, constructing a data clock generator from an oscillator, transistors, and logic gates was well known in the art at the time of the invention. That knowledge, supplemented with the specification, enables one of ordinary skill to construct the specific data clock generator of claim 14, which recites an input port, a divisor generator, and a binary divider. The divisor generator is specifically described at page 12, lines 17-26 for specific X and Y codes, with all possible divisors N_c shown in Figure 6. The divisor generator may calculate one of these values (e.g., the AND gate 3B6 of Fig. 3A, see page 13, lines 23-26), or may access them from a memory that stores the entire table and is accessible by the IC. The binary divider of the data clock generator recited in claim 14 is merely division circuitry (see Fig. 3BA, element 3B8), and it is asserted that one skilled in the art at the time of the invention would be enabled to construct division circuitry that is coupled and that resets as recited in claim 14.

As to claim 18, it is amended herein to recite that the program of instructions generate an aggregate PN code and receive an input from a PN master clock. The aggregate PN code is defined at page 11, lines 23-28, and generating it is described in Figure 3A (elements 3B2-3B5) and related text. Other elements of claim 18 are similarly taught as detailed above with respect to claim 14. One skilled in writing computer code for wireless telecommunication would be able to write a program that reads on claim 18, and embody it on a program storage device such as a ROM of a wireless radio, given ordinary skill as informed by the present specification. The term VHSIC Hardware Description Language (VHDL) file of claim 18 is

a term of art known to software programmers as a specific language type typically used for high speed ICs, such as high performance radios, software defined radios, and imaging arrays where data is processed in real time or very nearly real time.

None of claims 14-19 are seen to require undue experimentation, and the Office Action is not seen to recite reasons why any of those claims might not enable one of ordinary skill to make or use the claimed invention, as required under MPEP § 2164.04. The specification is seen to be enabling as provided at MPEP § 2164.05(b). The Applicant contends that the enablement rejection is unwarranted when ordinary skill in the art is considered. MPEP § 608.01(b) confirms that “Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described, and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail.” The circuitry and software programming detailed above is asserted to be within ordinary skill in the art, as informed by the written description.

The following parenthetical citations refer to the written description. The present application describes a way to avoid use of a symbol synchronizer, which is both an expensive component and difficult to make reliable over a wide range of symbol rates (page 3, lines 7-20). The present invention uses a PN code’s epochs (the boundaries at which components of the overall PN code repeats, typically their all-one’s state) to identify symbol boundaries (page 4, lines 6-8). For example, if XY epochs are used, it is always known that symbol boundaries occur at XY epochs. There are a number of chips per XY epoch, that number being X times Y (the number of chips per X epoch times the number of chips per Y epoch). It is desirable to have that number (the product XY) as rich in multiplicands as possible. With more relatively prime numbers comes a larger number of possible divisors and a larger number of possible symbol rates (data rates). A component code with a power of two length offers octave (power of two) data rates (page 2, lines d28-30). A companion component code rich in multiplicands offers not only more than the number of octave rates, it offers sub-octave rates (meaning a large and diverse variety of data rates) (page 2, line 30 to page 3, line 6).

Assume an overall PN code from three component codes, X (length that repeats every 4 chips), Y (length that repeats every 15 chips) and Z (length that repeats every 31 chips) (page 11, lines 23-28). These can be considered code lengths. Further assume six chips per symbol and a chipping rate of 60 Mc/s (mega-chips/second). The overall PN code then repeats every 1860 chips ($X*Y*Z$). An XY epoch is any epoch where both the X code and the Y code repeat, every 60 chips in this example. Each of those XY epochs also represents a symbol boundary, because 60 chips equals 10 symbols. There exists a set of integer divisors into the overall code length 1860 that yields another integer (page 12, lines 8-12), which in this example is the divisor set {1, 2, 3, 4, 5, 6, 10, 12, 15, 20, 30 and 60}. The X component code is length $2^n=2^2=4$ (page 12, lines 12-13). The Y component code is rich in multiplicands (3 and 5, which is also rich in prime numbers in this instance) (page 12, lines 13-15). The data rate is then [60 chips/XY epoch] *[1 symbol/divisor value]*[1 XY epoch/1 μ s], yielding data rates of 60, 30, 20, 15, 12, 10, 6, 5, 4, 3, 2, and 1 Msymbols/s for the respective divisor values of the divisor set above.

The symbol synchronizer becomes unnecessary because as soon as the X and Y component codes are detected and tracked, XY epochs are known, which means that symbol boundaries are known. That this is possible over a wide range of data rates (60:1 in the example) is a substantive advantage over using symbol synchronizers (page 9, line 28 to page 10, line 3). The “logarithmic division step size” makes possible a wide range of data rates within a smaller stored set of rates (page 12, lines 28-32). The above is seen to show that the claims read in view of the written description enables one of ordinary skill in the art to practice each and every claim.

The Examiner has rejected claims 1-20 under 35 USC § 112, second paragraph, for indefiniteness. Claims 1 and 18 are amended to more closely align the preamble and an element of the claim. The § 112, second paragraph rejection for the phrase “k is predetermined” of claims 3, 8, 14 and 20 is not understood. As described at page 12, line 1, $n=0, 1, 2, 3, \dots \text{max}$. The term k in these claims represents an upward bound to the variable n, which describes the size of the binary PN subcomponent codes as 2^n . As is known in the art, a spread spectrum receiver uses the same PN code as used by the transmitter, in order to be able to resolve the intended signal from noise. Because the PN code itself is ‘predetermined’

in the transmitter and receiver in order to intelligibly send and receive signals, the length of that overall PN code and any subcomponent codes from which the overall PN code derives must also be predetermined. Without an upward bound on n , the PN code would appear to have an indeterminate length.

Respecting claims 5 and 6, the Examiner asserts that the recited “step relationship” is indefinite. Generating the PN master clock divisor N_c according to a predetermined step relationship is detailed at page 12, lines 28 through page 13, line 8, and Figures 6-7. The step relationship between one divisor N_c and the next is predetermined by the value of the particular divisor N_c , as tabulated in Figure 6 that serves as the basis for the following examples. When N_c is below 10, each successive divisor (N_c+step) is one greater than the previous, hence a step size of one. When N_c is 320, the step size is 64 and the step relationship to achieve the next successive divisor is $+64$, yielding $N_c+step = 320+64 = 384$ as the next divisor. Data rates may be adjusted per page 13, lines 12-21 according to the step relationship. The relationship is predetermined because only one set of step relations follows for any values of n and m . Those values are recited in claims 3 and 4, from which claims 5 and 6 depend. As recited at page 12, lines 28-32, only some of the divisors listed in Figure 6 are required to obtain the full set. Those few retained divisors exhibit a log-linear relation with one another, as shown in Figure 7. Thus, knowing that the next successive divisor (or any other divisor) varies according to a log-linear function of a known divisor enables one to generate a PN master clock divisor according to that known or predetermined log-linear relation, as recited in claim 6. The present invention shows that knowing the values of n and m , as the receiver must in order to separate the spread spectrum signal from noise, imputes knowledge of the step-relation or log-linear step relation between successive divisors.

Claims 11, 12 and 13 are amended to address the rejection under 35 USC § 112, second paragraph, and draw support from Figure 3A.

Claim 19 is amended to properly place the acronym VHDL following the expanded term to which it relates. VHDL refers to VHSIC Hardware Description Language, where VHSIC is previously expanded in claim 19.

Claims 21-22 are added herein and draw support from claims 14 and 18, respectively.

Appl. No. 10/085,610
Amdt. Dated March 10, 2005
Reply to Office Action of December 14, 2004

The Applicant has sought to adopt as many of the Examiner's suggestions as possible without curtailing the scope of the claimed subject matter. Other matters are deemed to meet patentability criteria, and reasoning for retaining certain claim terms is detailed above. This response is seen to address each and every one of the objections and rejections in the outstanding Office Action, and the Applicant respectfully requests that the Examiner withdraw the objections and rejections, and pass claims 1-20 to issue without further delay. The undersigned welcomes the opportunity to resolve any remaining matters via teleconference at the Examiner's discretion.

Respectfully submitted:


Gerald J. Stanton

Reg. No.: 46,008

March 10, 2005

Date

Customer No. 29683
HARRINGTON & SMITH, LLP
4 Research Drive
Shelton, CT 06484-6212
Phone: (203) 925-9400
Facsimile: (203) 944-0245
Email: gstanton@hspatent.com

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

March 10, 2005
Date


Ann Okrentowich

AMENDMENTS TO THE DRAWINGS:

Nine drawing sheets of formal drawings are submitted herein to replace those informal drawings filed with the application. Of those nine sheets, four are labeled “Replacement page”, corresponding to Figures 1, 2A, 3A/3C, and 3B (Figures 3A and 3C being on one sheet).

In Figure 1, the block labeled “receiver” is given the reference number 14c, as recited at page 9, line 22 of the written description.

In Figure 2A, block elements 21 and 25 are now respectively labeled “PN Master Clock” and “Modulo-2 Combiner” per the Examiner’s comments.

In Figure 3A, the block element reciting “Reset ÷ Nc binary divider” is given reference number 3B8, as at page 12, line 8.

In Figure 3B, reference numbers are changed as follows:

31 is changed to 3B1;
321 is changed to 3B2;
323 is changed to 3B3;
324 is changed to 3B4;
327 is deleted;
322 is changed to 3B5;
325 is changed to 3B6; and
326 is changed to 3B8.

These changes to Figure 3B relate the blocks of Figure 3B to the functional blocks of Figure 3A by common reference numbers, and is supported by similar text descriptions within each block element of Figure 3B, and at page 7, lines 23-24 of the written description, which recites that Figure 3B is an integrated circuit incorporating features of the present invention.